REMARKS

Rejections under 35 U.S.C. § 103

The examiner rejected claims 1-4, 8-13, 17, 20-24, 26, 33, 36, 38-42, 45, 46, and 49 under 35 U.S.C. § 103(a) as being unpatentable under U.S. Patent No. 6,741,258 ("Peck") in view of U.S. Patent No. 6,085,296 ("Karkhanis") and further in view of U.S. Patent No. 5,956,754 ("Kimmel").

Specifically, the examiner contends that, with respect to Peck:

> **...according to the broadest reasonable interpretation given to the pending claims, since interface units are in charge of virtual to physical address translation, these interface units can be said to correspond to the claimed virtual interface.**

Applicants do not concede that the interface units of Peck can correspond to the virtual interfaces of the instant claims. Nevertheless, Applicants have amended independent claims 1, 17, 26, 33, 36, 42, and 46 to clarify the concept of a virtual interface.

Claim 1 recites "posting a descriptor, the descriptor comprising a virtual address in the first virtual memory address space and the shortcut, to a queue within a virtual interface that resides in a shared memory, between the first process and a second process, wherein the second process is in a second virtual memory address space that is different from the first virtual memory address space... notifying the second process that the descriptor has been posted to the queue via a notifying mechanism within the virtual interface ..."

Peck, in contrast, discloses the following with respect to interface units:

> **Interface units 22, which are separately designated with reference numerals 22a, 22b, 22c, and 22d, each function to support an interface between main memory device 14 and a specific processing device connected to memory control/interface device 12 by a respective bus. Each such bus allows the respective processing device to access main memory device 14 for the storage and retrieval of data and information...**
>
> **Each interface unit 22 comprises a separate translation look-aside buffer (TLB) 28. In particular, interface units 22a, 22b, 22c, and 22d include translation look-aside buffers 28a, 28b, 28c, and 28d, respectively.** [1]

[1] Peck, Column 4, Lines 33-53

Peck describes the interface units as including a means of support for an interface between a main memory device and a processing device connected via a bus, and a translation look-aside buffer (TLB). Nowhere does Peck describe or suggest a queue or mechanism for a first process to notify a second process about the posting of a descriptor within the interface unit.

Peck then further describes:

> **GART [Graphics Address Remapping Table] walk device 24 receives the various requests from translation look-aside buffers 28 and then arbitrates to determine an order for processing the requests. GART walk device 24 then performs the GART walk process for each request according to the determined order. In the GART table walk process, information is retrieved from page directory 18 and/or page tables 20 for use in translating a virtual linear address into a physical address.**
>
> **The information for performing a translation is brought into the respective translation look-aside buffer 28 (via GART table walk device 24 and memory controller 26). The respective interface unit 22 then uses the information to translate the virtual address into a physical address. Once the physical address has been derived, it is used to access the data desired by the respective processing device.** [2]

That is, the GART walk device, which is connected to all the TLBs from the interface units, takes the requests, prioritizes them, and, in order, gets the information for each request for translating a virtual linear address into a physical address. The translation is performed within each respective interface unit.

Assume, *arguendo*, that the requesting represents a first process and the translation a second process. The interface between the first process and the second process, where notification that a request has been made occurs, takes place in the GART walk device and not in an interface unit. The GART walk device, however, is not a virtual interface, as it does not reside in a shared memory. Thus, neither the interface units nor the GART walk device describes or suggests or is equivalent to the claimed virtual interfaces.

Karkhanis fails to cure the deficiencies of Peck. The examiner admits that: "**Peck does not explicitly disclose the details of 'determining, by the second process, the physical address corresponding to the virtual address based on at least the virtual address associated with the first process and the shortcut.'**" The examiner relies on Karkhanis for this teaching. Karkhanis describes a "global section" as "a section [i.e., collection of physical pages managed as a group by an operating system] that can be

[2] Peck, Column 5, Line 66 – Column 6, Line 5 and FIG. 2

simultaneously shared in several processes' address spaces"[3]. The examiner also argues that: "**and *applicant should note that according to the broadest reasonable interpretation given to the pending claims, since interface units are in charge of virtual to physical address translation, these interface units can be said to correspond to the claimed virtual interface.***" Applicant contends that this interpretation is incorrect. Karkhanis also states:

> **...the management of a global section uses several basic data structures that are stored in system address space. For historical reasons, each global section is managed by two data structures: a Global Section Descriptor (GSD) 400, and an entry in the Global Section Table, a Global Section Table entry (GSTE) 500. For each global section, these two data structures, and their associated PTE's, have fields (either pointers or table index values) that maintain their association with each other...the second data structure describing a global section is a Global Section Table entry (GSTE) 500. Each GSTE contains, among other things, a pointer 502 to the corresponding GSD 400, a flags field 504 (whose contents are the same as the flags field 404 of the corresponding GSD), a reference counter 508 used for GSTE accounting purposes (the number of process Page Table Entries (PTE's) that map to pages within the global section), a count of the number of pages in the global section and information about the file that is used as the backing storage for the pages within the global section. The GSTE also contains an index 512 into the Global Page Table (GPT) of the first Global Page Table Entry (GPTE) corresponding to this global section.[4]**

A global section, then, is made up of a GSD and a GST, the GST having entries, each entry containing a pointer to the GSD, flags, a reference counter, and file information. None of these data structures, however, include a queue, or a mechanism for a first process to notify a second process about the posting of a descriptor as recited in claim 1. Therefore, Karkhanis cannot suggest the feature of the virtual interface

Kimmel fails to cure the deficiencies of Peck and Karkhanis. Kimmel describes the following:

> **FIG. 3 shows the dynamically mapped shared memory (DSHM). Task 1 and task 2 each have a logical address space 310 and 320. These are mapped to the shared map slots 330 which allow the tasks to access all of shared memory 340. Each task maps a number of buffers using slots in map 330. For example, Task 1 has a location 301 in its address space that is mapped via map slot 303 to a piece of shared memory 304. Task 2 is also mapping the same piece of shared memory 340 at the same address in its**

[3] Karkhanis, Column 6, Lines 49-55
[4] Karkhanis, Column 13, Lines 24-65

> **address space at 302. If Task 1 reference a location in 301 the memory reference goes to physical memory 304 in shared object 340. Task 2 can reference the same physical memory using the mapping at 302.**[5]

The examiner equates the shared map slots 330 with a virtual interface. The shared map slots, however, are filled with maps between task addresses and shared memory locations, for example. Nowhere does Kimmel describe these slots as containing a queue or a mechanism for a first process to notify a second process about the posting of a descriptor as recited in claim 1.

Peck, Karkhanis, and Kimmel, alone or in combination, neither describe nor suggest at least the feature of "posting a descriptor, the descriptor comprising a virtual address in the first virtual memory address space and the shortcut, to a queue within a virtual interface that resides in a shared memory, between the first process and a second process, wherein the second process is in a second virtual memory address space that is different from the first virtual memory address space…notifying the second process that the descriptor has been posted to the queue via a notifying mechanism within the virtual interface…" recited in claims 1-4, 8-13, 17, 20-24, 26, 33, 36, 38-42, and 46. Further, claims 45 and 49 have been cancelled. Accordingly, Applicants request that the rejection be withdrawn.

The examiner rejected claims 5-7, 14-16, 18, 19, 25, 27, 28, 34, 35, 37, 43, 44, 47, and 48 under 35 U.S.C. § 103(a) as being unpatentable under Peck in view of Karkhanis and Kimmel, and further in view of U.S. Patent Application Publication No. 2003/0204648 ("Arndt").

Claims 5-7, 14-16, 18, 19, 27, 28, 34, 35, 37, 43, 44, 47, and 48 depend from independent claims 1, 17, 26, 33, 36, 42, and 46, with claim 25 having been cancelled. Applicants have shown *supra* that Peck, Karkhanis, and Kimmel, alone or in combination, neither describe nor suggest at least the feature of "posting a descriptor, the descriptor comprising a virtual address in the first virtual memory address space and the shortcut, to a queue within a virtual interface that resides in a shared memory, between the first process and a second process, wherein the second process is in a second virtual memory address space that is different from the first virtual memory address space…notifying the second process that the descriptor has been posted to the

[5] Kimmel, Column 4, Lines 31-44

queue via a notifying mechanism within the virtual interface…" recited in claims 1-4, 8-13, 17, 20-24, 26, 33, 36, 38-42, and 46.

Arndt fails to cure the deficiencies of Peck, Karkhanis, and Kimmel. Arndt was presented as a reference by the examiner in order to illustrate a function/key used to encrypt a shortcut, where the encryption is unknown to a first process and only a second process is capable of decryption. Nowhere does Arndt describe or suggest a virtual interface between a first process and a second process such that the virtual interface resides in shared memory and includes a queue, and a mechanism for a first process to notify a second process about the posting of a descriptor as recited in claim 1.

Peck, Karkhanis, Kimmel, and Arndt, alone or in combination, neither describe nor suggest at least the feature of "posting a descriptor, the descriptor comprising a virtual address in the first virtual memory address space and the shortcut, to a queue within a virtual interface that resides in a shared memory, between the first process and a second process, wherein the second process is in a second virtual memory address space that is different from the first virtual memory address space…notifying the second process that the descriptor has been posted to the queue via a notifying mechanism within the virtual interface…" recited in claims 5-7, 14-16, 18, 19, 27, 28, 34, 35, 37, 43, 44, 47, and 48. Accordingly, Applicants request that the rejection be withdrawn.

It is believed that all the rejections and/or objections raised by the examiner have been addressed.

In view of the foregoing remarks, applicant respectfully submits that the application is in condition for allowance and such action is respectfully requested at the examiner's earliest convenience.

All of the dependent claims are patentable for at least the reasons for which the claims on which they depend are patentable.

Canceled claims, if any, have been canceled without prejudice or disclaimer.

Any circumstance in which the applicant has (a) addressed certain comments of the examiner does not mean that the applicant concedes other comments of the examiner, (b) made arguments for the patentability of some claims does not mean that there are not other good reasons for patentability of those claims and other claims, or (c) amended or canceled a claim

does not mean that the applicant concedes any of the examiner's positions with respect to that claim or other claims.

No fee is due. Please apply any other charges or credits to deposit account 06-1050.

Respectfully submitted,

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